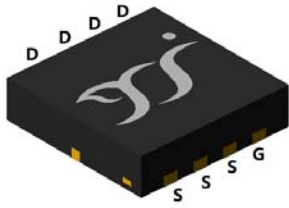
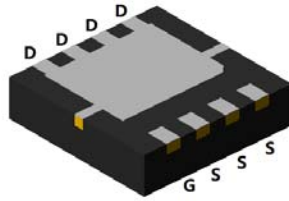


N-Channel Enhancement Mode Field Effect Transistor

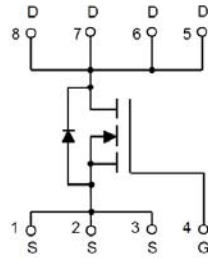


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 60V
- I_D 18A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<30m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<40m\Omega$
- 100% EAS Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter
- 12V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ C$	I_D	18	A
	$T_C=100^\circ C$		11	
	$T_A=25^\circ C$		5.7	
	$T_A=100^\circ C$		3.6	
Pulsed Drain Current ^A		I_{DM}	60	A
Avalanche energy ^B		EAS	72	mJ
Total Power Dissipation ^C	$T_C=25^\circ C$	P_D	18.5	W
	$T_C=100^\circ C$		7.4	
	$T_A=25^\circ C$		2	
	$T_A=100^\circ C$		0.8	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	6.7	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	60	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ18N06AQ	F1	Q18N06A	5000	10000	100000	13" reel



YJQ18N06AQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	23	30	mΩ
		V _{GS} =4.5V, I _D =10A	-	26	40	
Diode Forward Voltage	V _{SD}	I _S =18A, V _{GS} =0V	-	0.85	1.2	V
Gate resistance	R _G	f=1MHz	-	1	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	1200		pF
Output Capacitance	C _{oss}		-	70		
Reverse Transfer Capacitance	C _{rss}		-	60		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =18A	-	23	-	nC
Gate-Source Charge	Q _{gs}		-	3	-	
Gate-Drain Charge	Q _{gd}		-	6	-	
Reverse Recovery Charge	Q _{rr}	I _F =18A, di/dt=100A/us	-	17.5	-	nC
Reverse Recovery Time	t _{rr}		-	23.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _{DS} =18A	-	5	-	ns
Turn-on Rise Time	t _r		-	45	-	
Turn-off Delay Time	t _{D(off)}		-	19	-	
Turn-off fall Time	t _f		-	2	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=40V, V_G=10V, L=0.5mH, I_{AS}=17A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design..



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Typical Electrical and Thermal Characteristics Diagrams

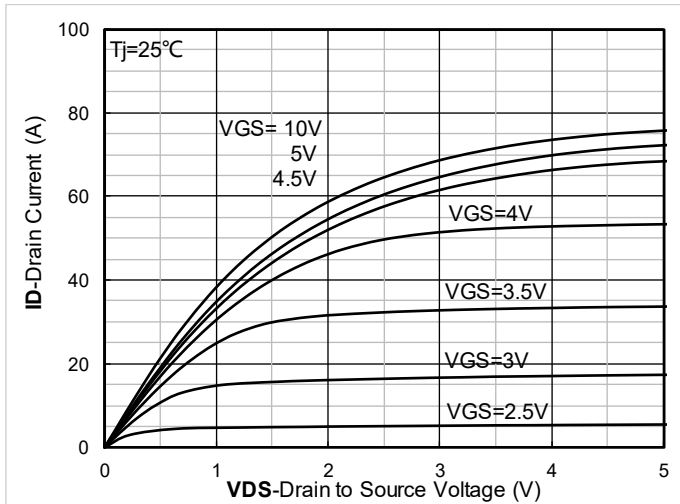


Figure 1. Output Characteristics

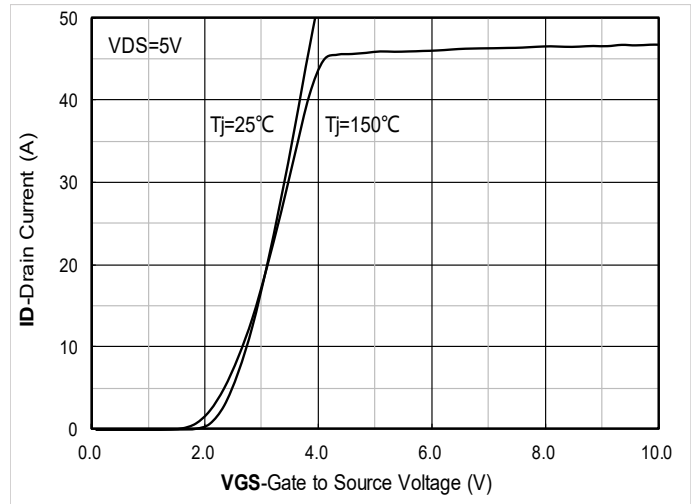


Figure 2. Transfer Characteristics

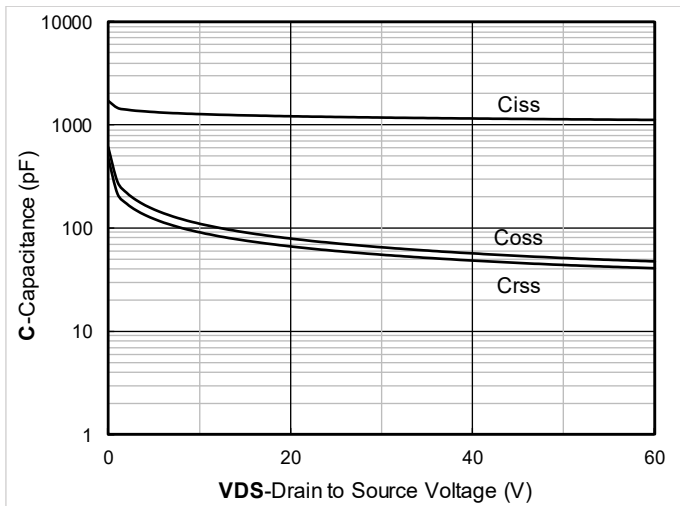


Figure 3. Capacitance Characteristics

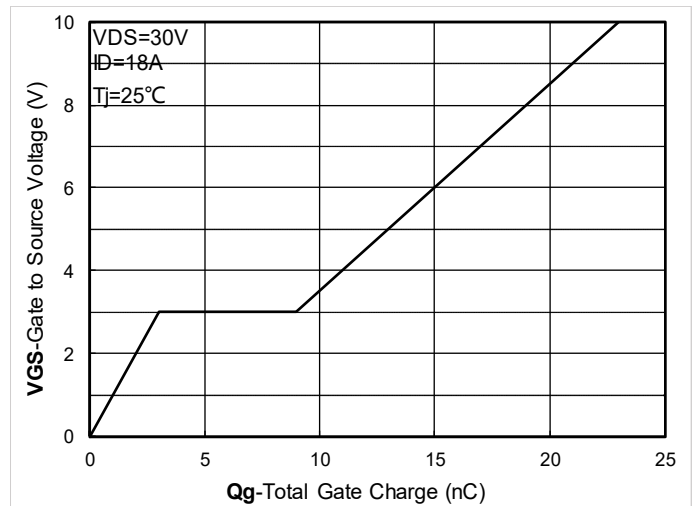


Figure 4. Gate Charge

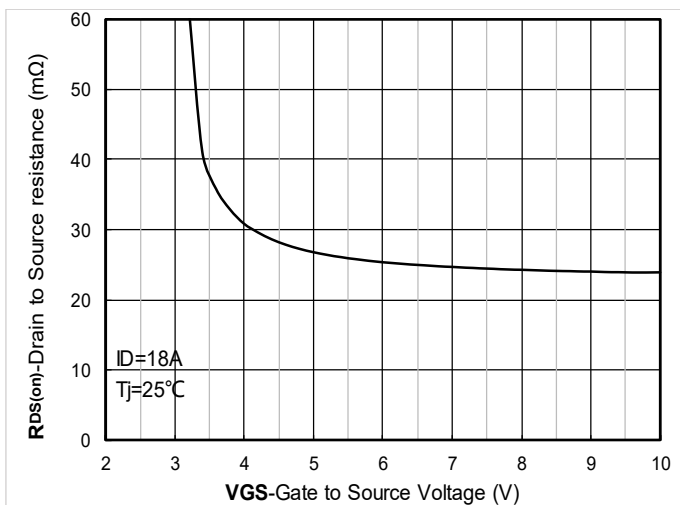


Figure 5. On-Resistance vs Gate to Source Voltage

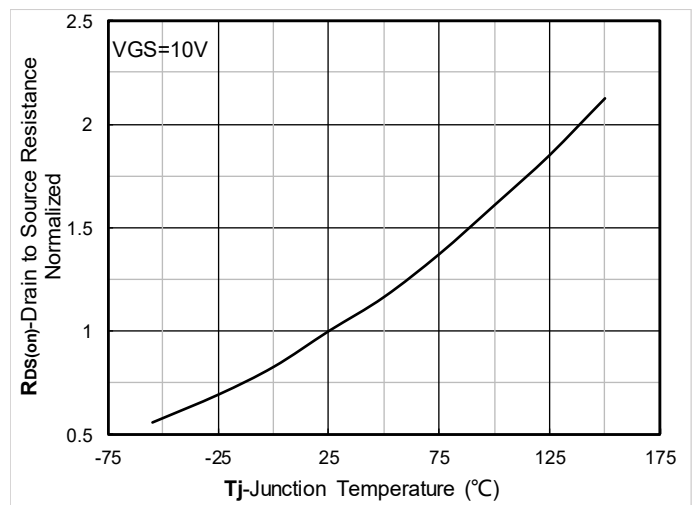


Figure 6. Normalized On-Resistance



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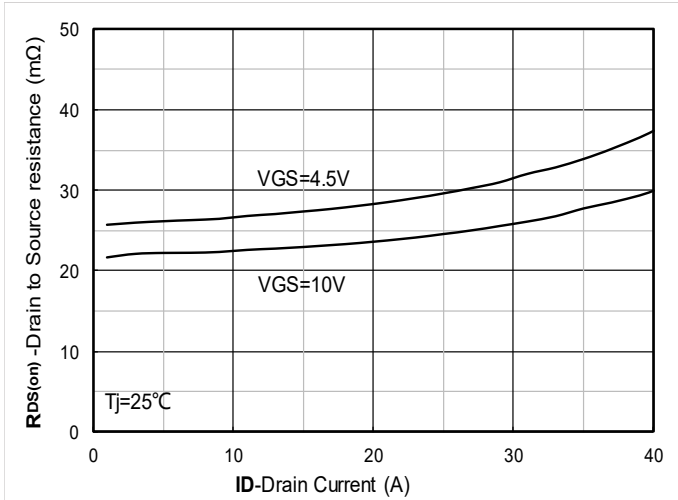


Figure 7. $R_{DS(on)}$ VS Drain Current

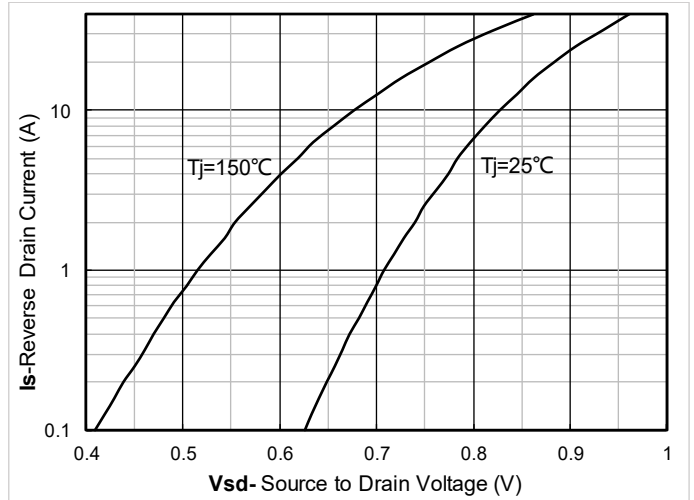


Figure 8. Forward characteristics of reverse diode

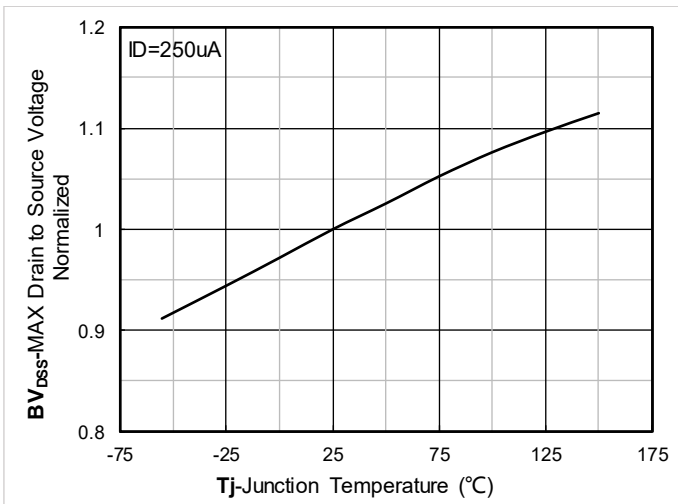


Figure 9. Normalized breakdown voltage

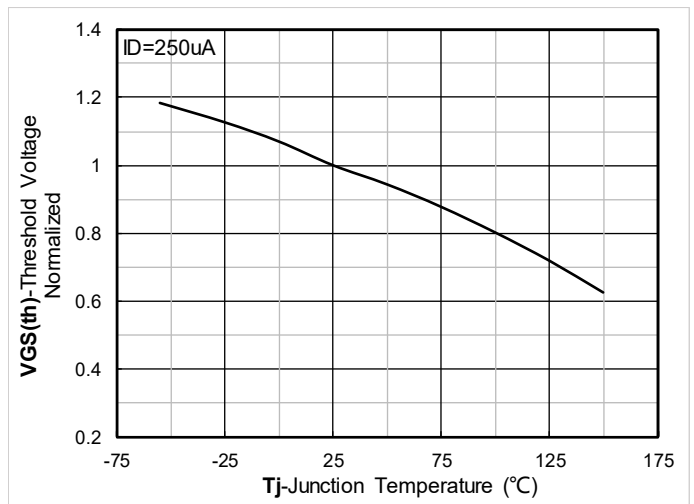


Figure 10. Normalized Threshold voltage

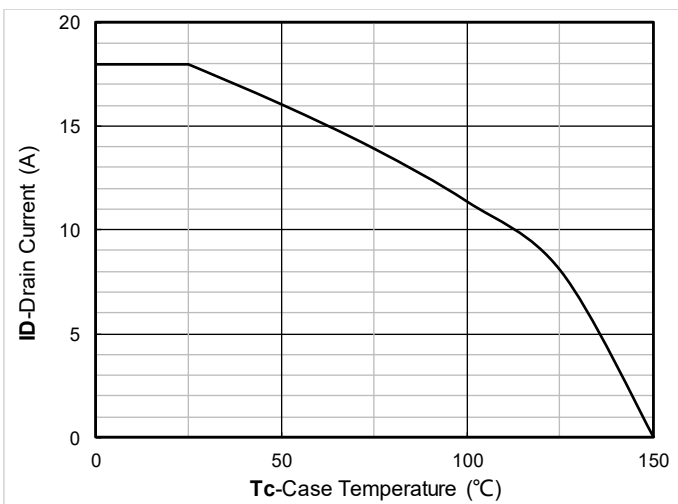


Figure 11. Current dissipation

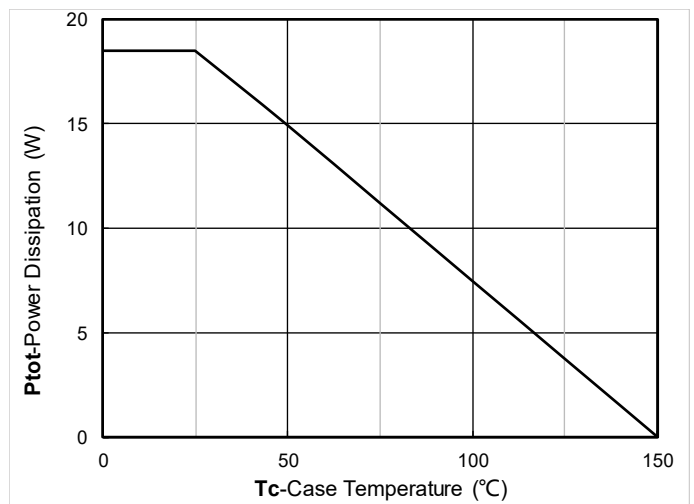


Figure 12. Power dissipation



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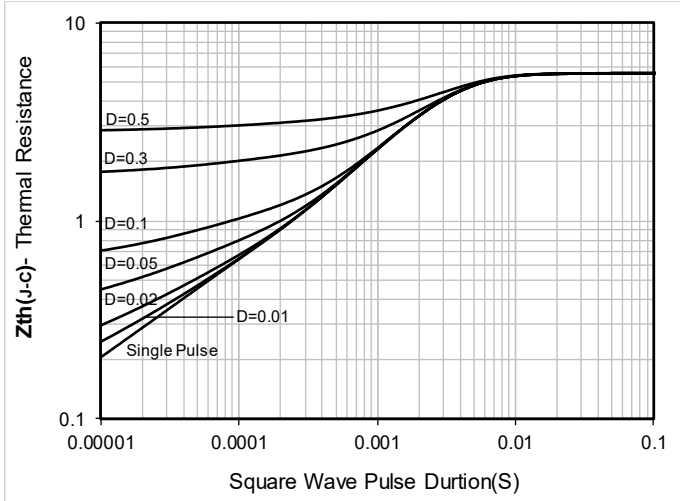


Figure 13. Maximum Transient Thermal Impedance

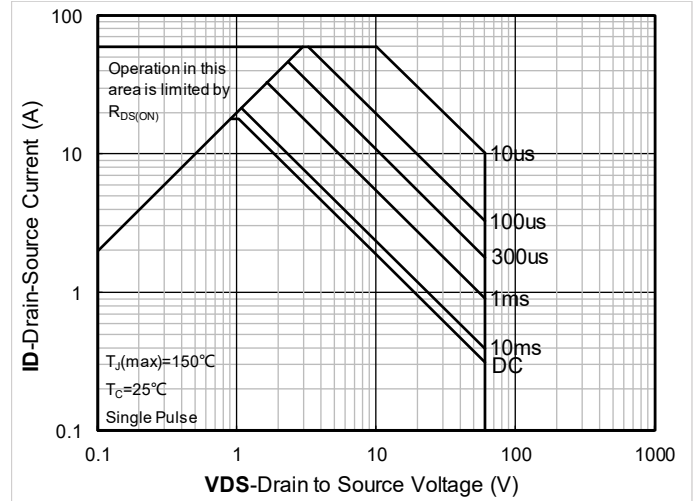
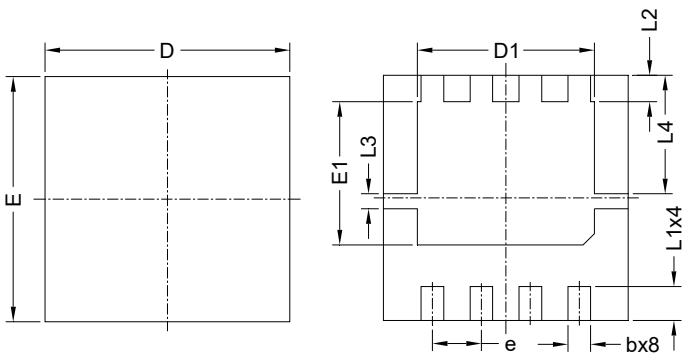


Figure 14. Safe Operation Area



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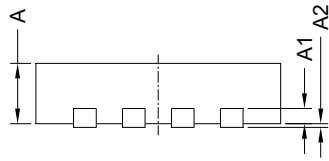
DFN3333-8L Package information



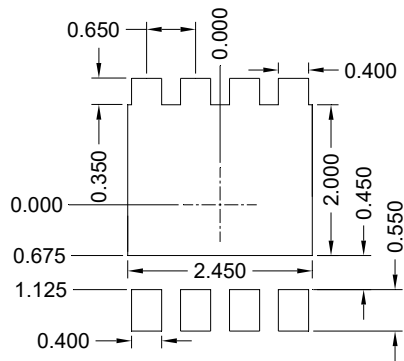
Top View
正面视图

Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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Rev	Date	Modify content
1.0	30-Jun-23	New datasheet